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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,353	01/23/2004	Randy Hoffman	200311332-2	7102
22879	7590	06/07/2006	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			MONDT, JOHANNES P	
			ART UNIT	PAPER NUMBER
			3663	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/763,353

Applicant(s)

HOFFMAN ET AL.

Examiner

Johannes P. Mondt

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4,6-9,11,12,14,15,19,21-24,26,29 and 31-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 4,6-9,11,12,14,15,19,21-24,26,29 and 31-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>5/5/6, 5/8/6</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

Amendment filed 5/17/06 After Final Rejection forms the basis for this office action. In said Amendment applicant canceled claims 1-3, 5, 10, 13, 16-18, 20, 25, 27, 28, 30, 40-43, 45-47 and 49 and amended claims 4, 6-9, 11, 12, 14, 19, 21-24, 26, 29, 31-38 and 48.

Carcia et al (IDS filed 5/8/06 and sent as "a further reference" May 4, 2006) appears to be a pertinent reference to subject matter previously indicated as allowable, with regrets by examiner.

In view Carcia et al the finality of the office action mailed 3/20/06 is herewith withdrawn.

Comments on Remarks made in said Amendment are included below under "Response to Arguments".

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statements (IDS) filed 5/5/06 and 5/8/06. Signed copies of Forms PTO-1449 are included for both IDS documents with this office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

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applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 4, 6-9, 11, 26, 29, 31-36 and 48** are rejected under 35 U.S.C. 102(e) as being anticipated by Carcia et al (US 2004/0127038 A1).

Carcia et al teach a semiconductor device (thin film transistor; see title), comprising: a source electrode ("Source", Figure 3, also: inherent in thin film transistor); a drain electrode ("Drain", Figure 3, equally inherent on thin film transistor), a channel coupled to the source and drain electrode (zinc oxide comprising semiconductor layer; see Figure 3 and [0042]; said channel also is inherent in any thin film transistor) and comprised of a ternary compound containing zinc, tin and oxygen (see [0010]), where at least a portion of the channel is formed from a zinc-tin oxide compound having the stoichiometric formula Zn_2SnO_4 (namely: one of said "combinations", especially the combination $2\text{ZnO} + \text{SnO}_2 \rightarrow \text{Zn}_2\text{SnO}_4$); and a gate electrode ("Gate" in Figure 3; equally inherent in any thin film transistor) configured to permit application of an electric field to the channel (which is the very function of a gate).

On claim 6: the limitation "substantially amorphous" is met by Carcia et al, because inherently sputtering creates substantially amorphous forms of zinc oxide based oxides, as witnessed for example by Henrichs (US 2003/0185266 A1) ([0046], not cited here other than for establishment of fact).

On claim 7: one or more of the source, drain and gate electrodes are fabricated so as to be at least partially transparent (all of gate, drain and source electrodes are made of transparent zinc oxide; see Example 7, [0053]).

On claims 8-9: the limitations of claims 8 and 9 are met by virtue of the finite dissociation constant of Zn_2SnO_4 . For the finiteness of said dissociation constant the examiner takes official notice.

On claim 11: The limitation "is adapted to be deposited using an RF sputtering process", is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al*, 218 USPQ 289, 292 (Fed. Cir. 1983), and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

In the underlying case it is therefore only parenthetically mentioned that indeed the channel of the prior art is adapted to be deposited using RF sputtering ([0010] and [0047]).

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On claim 29: Carcia et al teach a thin film transistor([010] and [0031]-[0055]), comprising: a gate electrode ("Gate", Figure 3), a channel layer from a zinc-tin oxide material (namely: Zn_2SnO_4 among other) (the ZnO base semiconductor layer comprises a channel in operation, hence is a channel layer); a dielectric material disposed between and separating the gate electrode and the channel layer (SiO_2 layer in Figure 3); first and second electrodes as claimed being met by the source ("Source"; Figure 3) and drain ("Drain") electrodes and disposed adjacent the channel layer on a side of the channel layer opposite the dielectric material, such that the channel layer is disposed between and electrically separates the first and second electrodes (thus far this claim limitation merely recites inherent properties of a thin film transistor with insulated gate), where at least a portion of the channel layer is formed from a zinc-tin oxide compound having the stoichiometry Zn_2SnO_4 ([0010]).

On claim 26: the examiner takes official notice that the limitation defined by this claim is inherently met, by any thin film transistor by definition of its gate.

On claim 31: the limitation "substantially amorphous" is met by Carcia et al, because inherently sputtering creates substantially amorphous forms of zinc oxide based oxides, as witnessed for example by Henrichs (US 2003/0185266 A1) ([0046], not cited here other than for establishment of fact).

On claim 32: one or more of the source, drain and gate electrodes are fabricated so as to be at least partially transparent (all of gate, drain and source electrodes are made of transparent zinc oxide; see Example 7, [0053]).

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On claims 33-34: the limitations of claims 8 and 9 are met by virtue of the finite dissociation constant of Zn_2SnO_4 . For the finiteness of said dissociation constant the examiner takes official notice.

On claim 35: one or more of the source, drain and gate electrodes are fabricated so as to be at least partially transparent (all of gate, drain and source electrodes are made of transparent zinc oxide; see Example 7, [0053]).

On claim 36: The limitation "is adapted to be deposited using an RF sputtering process", is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al*, 218 USPQ 289, 292 (Fed. Cir. 1983), and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the underlying case it is therefore only parenthetically mentioned that indeed the channel of the prior art is adapted to be deposited using RF sputtering ([0010] and [0047]).

On claim 48: Carcia et al teach a display (their claim 16) comprising: a plurality of display elements configured to being capable to operate collectively to display images,

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wherein each of the display elements includes a semiconductor device configured to control light emitted by the display element (namely: the transparent oxide semiconductor transistors; see their claim 16), the semiconductor device including: a source electrode ("Source", Figure 3, also: inherent in thin film transistor); a drain electrode ("Drain", Figure 3, equally inherent on thin film transistor), a channel coupled to the source and drain electrode (zinc oxide comprising semiconductor layer; see Figure 3 and [0042]; said channel also is inherent in any thin film transistor) and comprised of a ternary compound containing zinc, tin and oxygen (see [0010]), where at least a portion of the channel is formed from a zinc-tin oxide compound having the stoichiometric formula Zn_2SnO_4 (namely: one of said "combinations", especially the combination $2ZnO + SnO_2 \rightarrow Zn_2SnO_4$); and a gate electrode ("Gate" in Figure 3; equally inherent in any thin film transistor) configured to permit application of an electric field to the channel (which is the very function of a gate).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. ***Claims 19, 21, 22 and 24*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Carcia et al (US 2004/0127038 A1) in view of Taylor (4,521,698).

On claim 19: Carcia et al teach a three-port device (source, drain and gate being the three ports), comprising: a source electrode ("Source"; Figure 3); a drain electrode ("Drain"; cf. Figure 3); a gate electrode ("Gate"; Figure 3); furthermore, in reference to the claim limitation "means for providing a channel configured to permit movement of electric charges there-through between the source electrode and the gate electrode, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

In the underlying case, it is thus only parenthetically mentioned that indeed the prior art by Carcia et al teaches a means for providing channel disposed between the source electrode and the drain electrode (said means being a semiconducting oxide layer comprising zinc separating source and channel with a gate electrode sufficiently nearby to produce a channel when given a voltage that either accumulates, depletes or inverts the interface between the semiconducting oxide layer and a dielectric layer separating gate from semiconductor oxide layer; furthermore, channel is inherent in the thin film transistor by Carcia et al and is implied by the existence of a gate near a channel forming substance, as the ZnO area in Figure 3), inherently permitting movement of electric charge there-through between source and drain in response to a voltage applied at the gate electrode, the means for providing a channel formed at least in part from a ternary compound

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containing zinc, tin and oxygen, where the means for providing a channel includes means for providing a semiconductor formed from a zinc-tin oxide compound having the stoichiometry Zn_2SnO_4 .

Also, the limitation "means for providing a semiconductor" (second line from below) constitutes a product-by-process limitation, because, while said channel comes about through a method of use (application of voltage to gate), the "means for providing a semiconductor is a limitation on how to make said semiconductor. The limitation is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al*, 218 USPQ 289, 292 (Fed. Cir. 1983), and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Carcia et al do not necessarily teach the limitation movement between source electrode and gate electrode rather than drain electrode. However, it would have been obvious to include said limitation in view of Taylor, who, in a patent on insulated gate field effect transistors, namely MOSFETs, hence related art, teach the

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use thereof wherein gate and drain are conductively connected so as to avoid hot electron effects (title, abstract, Figure 3; in particular transistor 224; and columns 1-3).

Motivation to include the teaching by Taylor at least derives from the generic undesirability of hot electron effects, i.e., effect whereby the acceleration of electrons due to the voltage head between source and drain leads to electron-electron collisions upon the impact on the drain region of accelerated electrons from the channel, resulting in the excitation of valence electrons into the conduction band, i.e., to electron-hole pair production, resulting, due to the relatively large effective mass of the holes, in unwanted further bias of the semiconductor region near the channel.

On claim 21: the limitation "substantially amorphous" is met by Carcia et al, because inherently sputtering creates substantially amorphous forms of zinc oxide based oxides, as witnessed for example by Henrichs (US 2003/0185266 A1) ([0046], not cited here other than for establishment of fact).

On claim 22: one or more of the source, drain and gate electrodes are fabricated so as to be at least partially transparent (all of gate, drain and source electrodes are made of transparent zinc oxide; see Example 7, [0053]).

On claim 24: the semiconductor device by Carcia et al further comprises a dielectric disposed between and physically separating the gate electrode from the semiconductor layer that provides the channel (SiO₂ layer in Figure 3). Furthermore, means for providing a dielectric" constitutes a product-by-process limitation, because

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said means is not a structural aspects but instead merely a means for providing, i.e., a means for making a structural component. The limitation is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting.

A product by process claim is directed to the product per se, no matter how they are actually made. See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al*, 218 USPQ 289, 292 (Fed. Cir. 1983), and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113.

Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

3. **Claims 12 and 37** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Carcia et al* as applied to claim 4, in view of *Hong et al* (6,674,495 B1).

As detailed above, *Carcia et al* anticipate claims 4 and 29. *Carcia et al* do not necessarily teach the further limitation that the source and drain electrodes are formed from an indium-tin oxide material. However, it would have been obvious to include this further limitation in view of *Hong et al*, who, in a patent on a thin film transistor array panel for display, hence analogous art (see title and abstract), teach the source and drain electrodes to be ITO (i.e., indium-tin oxide) electrodes (see column 20, lines 25-37, and e.g., Figures 1 and 23) in a patent in which ITO and zinc oxide are both *aequo* cited for conductivity and transparency, two important advantages for electrode

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material in a display (see, e.g., columns 9 and 20). Inherently, source and drain electrodes in any thin film transistor, in fact in any field effect transistor, are separate from one another. Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416. Furthermore, the limitations “formed from” and “patterned” constitute product-by-process limitations and are only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product “gleaned” from the process steps that must be determined in a “product-by-process” claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in “product by process” claims or not.

4. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Carcia et al and Taylor as applied to claim 19 above, and further in view of Hong et al (6,674,495 B1).

As detailed above, claim 19 is unpatentable over Carcia et al in view of Taylor.

Carcia et al nor Taylor necessarily teach the further limitation that the source and drain

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electrodes are formed from an indium-tin oxide material. However, it would have been obvious to include this further limitation in view of Hong et al, who, in a patent on a thin film transistor array panel for display, hence analogous art (see title and abstract), teach the source and drain electrodes to be ITO (i.e., indium-tin oxide) electrodes (see column 20, lines 25-37, and e.g., Figures 1 and 23) in a patent in which ITO and zinc oxide are both *ex aequo* cited for conductivity and transparency, two important advantages for electrode material in a display (see, e.g., columns 9 and 20). Inherently, source and drain electrodes in any thin film transistor, in fact in any field effect transistor, are separate from one another. Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416. Furthermore, the limitations "formed from" and "patterned" constitute product-by-process limitations and are only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new

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method is not a patentable product, whether claimed in "product by process" claims or not.

5. **Claims 14 and 38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Carcia et al in view of Krivokapic et al (6,100,558).

Carcia et al teach a semiconductor device (thin film transistor; see title), comprising: a source electrode ("Source", Figure 3, also: inherent in thin film transistor); a drain electrode ("Drain", Figure 3, equally inherent on thin film transistor), a channel coupled to the source and drain electrode (zinc oxide comprising semiconductor layer; see Figure 3 and [0042]; said channel also is inherent in any thin film transistor) and comprised of a ternary compound containing zinc, tin and oxygen (see [0010]), where at least a portion of the channel is formed from a zinc-tin oxide compound having the stoichiometric formula Zn_2SnO_4 (namely: one of said "combinations", especially the combination $2\text{ZnO} + \text{SnO}_2 \rightarrow \text{Zn}_2\text{SnO}_4$); and a gate electrode ("Gate" in Figure 3; equally inherent in any thin film transistor) configured to permit application of an electric field to the channel (which is the very function of a gate), where the gate electrode is physically separated from the channel by a dielectric material (SiO_2 ; see Figure 3).

Carcia et al do not necessarily teach the limitation that said dielectric material is an aluminum-titanium oxide material. However, it would have been obvious to include said limitation as witnessed, for instance, by Krivokapic et al, teaching a combination of Al_2O_3 and TiO_2 for the gate dielectric layer the purpose of increasing the dielectric constant of the gate oxide (Figure 19 and column 8, lines 3-26) so as to overcome adverse effects of small defects or contamination of the gate oxide material (see

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"Background of the Invention", col. 1). *Motivation* to include the teaching by Krivokapic et al in the invention by Carcia et al derives from the consequent reduction in defective operation.

On claim 38: Carcia et al teach a thin film transistor (title) comprising: a gate electrode (Figure 3, "Gate"; inherent in any thin film transistor), a channel layer comprising a zinc-tin oxide material (zinc oxide comprising semiconductor layer; see Figure 3 and [0042]; said channel also is inherent in any thin film transistor) (zinc oxide comprising semiconductor layer; see Figure 3 and [0042]; said channel also is inherent in any thin film transistor); a dielectric material (SiO₂ layer; Figure 3) disposed between and separating the gate electrode and the channel layer, and where first and second electrodes (Source and Drain electrodes; Figure 3) spaced from each other and disposed adjacent the channel layer on a side of the channel layer opposite the dielectric material (inherent to thin film transistor) such that the channel layer is disposed between and electrically separates the first and second electrodes (inherent, short of separation as claimed thin film transistor would not operate).

Carcia et al do not necessarily teach said dielectric layer to be an aluminum-titanium oxide layer. However, it would have been obvious to include said limitation as witnessed, for instance, by Krivokapic et al, teaching a combination of Al₂O₃ and TiO₂ for the gate dielectric layer the purpose of increasing the dielectric constant of the gate oxide (Figure 19 and column 8, lines 3-26) so as to overcome adverse effects of small defects or contamination of the gate oxide material (see "Background of the Invention",

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col. 1). *Motivation* to include the teaching by Krivokapic et al in the invention by Carcia et al derives from the consequent reduction in defective operation.

6. **Claims 15 and 39** are rejected under 35 U.S.C. 103(a) as being unpatentable over Carcia et al and Krivokapic et al as applied to claims 14 and 38, respectively, above, and further in view of Hornik et al (US 2004/0169210 A1).

As detailed above, claims 14 and 38 are unpatentable over Carcia et al in view of Krivokapic et al.

Neither Carcia et al nor Krivokapic et al necessarily teach the further limitation defined by claims 15 or 39, respectively.

*However, it would have been obvious to include said further limitation in view of Hornik et al, who, in a patent on barrier material against the diffusion of hydrogen into a high dielectric constant layer such as PZT during passivation of gate oxide, teaches to protect said layer of PZT with a pair of Al_2O_3 layers with a TiO_2 layer in between (see [0006] and [0024]). Because PZT is also included in the teaching by Krivokapic et al as one of the gate oxide materials, it would have been obvious to include the teaching on hydrogen diffusion barrier structure against deterioration of PZT also in the gate oxide by Krivokapic et al. To protect the PZT layer optimally it would furthermore have been obvious to provide the $\text{Al}_2\text{O}_3/\text{TiO}_2/\text{Al}_2\text{O}_3$ layer on both sides of the PZT layer, thus meeting the claim limitation. *Motivation* to include the teaching by Hornik et al derives immediately from the increased integrity resulting from the protection of the PZT against a lowering of its dielectric constant due to hydrogen diffusion.*

Response to Arguments

The Amendment proposed After Final Rejection and filed 5/17/06 has been entered in view of the Information Disclosure statement filed 5/8/06, listing Carcia et al as a further reference thus far not having been made of record; as evidenced from the rejections made above, Carcia et al is pertinent prior art, over which all claims in said proposed amendment have been rejected. Because secondary references were needed for some of the rejections the present office action has been made non-final.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM

June 2, 2006

Patent Examiner:

A handwritten signature in black ink, appearing to read 'Johannes Mondt', with a stylized flourish at the end.

Johannes Mondt (Art Unit: 3663).